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Comments

U.S. Patent Application No.: 10/729,457

SEMICONDUCTOR INTEGRATED CIRCUIT ...

Our Reference No.: NECE 20.780 (100806-00243)

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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

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Attorney Docket No.: NECE 20.780 (100806-00243)



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor : Minari Arai  
Title : SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE  
AND METHOD OF DETECTING DELAY ERROR IN  
THE SAME  
Serial No. : 10/729,457  
Confirmation No. : 1313  
Filed : 12/05/2003  
Examiner : Linh M. Nguyen  
Group Art Unit : 2816

Mail Stop: Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

April 7, 2005

**Comments on Statement of Reasons for Allowance**

Sir:

The referenced application was allowed on, January 21, 2005. The issue fee due on April 21, 2005 is being paid concurrently herewith.

Applicant hereby acknowledges the Examiner's Reasons for Allowance.

Applicant respectfully notes that there may be additional reasons for allowance that have not been specifically cited, and which may apply to various of the allowed claims, in addition to or

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instead of the cited reasons. Applicant respectfully suggests that notwithstanding the Examiner's Reasons for Allowance, it is believed that each of the allowed claims is patentable in its own right and/or for other reasons raised during the prosecution and/or explained in the specification of this application.

To the extent that any statements regarding patentability of any claims allowed by the Examiner made by the Applicant or the Examiner in any document filed in this application are inconsistent with or not included in the Examiner's Reasons for Allowance, they are incorporated by reference herein.

Any fee due with this paper may be charged on Deposit Account No. 50-1290.

Respectfully submitted,



Thomas J. Bean  
Reg. No. 44,528

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**Date: April 7, 2005**  
**Docket No.: NECE 20.780 (100806-00243)**

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